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Design and Synthesis of PDM/DP-QPSK/BPSK Transceiver

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Abstract: **In this paper we are going to design and synthesis of PDM/ DP-QSPK/BPSK Transceiver. All this techniques are very important in analog digital communication .These techniques can also implemented by using VHDL or VERILOG language. The digital system of QPSK is planned using a reversible logic gates which yields in low power, less required area and less amount of delay. These techniques can easily implemented on FPGA. Some simulation results of these techniques are also in presented in this paper.**

Keywords: **VHDL or VERILOG language, PDM/ DP-QSPK/BPSK.**

1. INTRODUCTION

In Quadrature phase shift keying modulation a sinusoidal waveform is varied in phase while keeping the amplitude and frequency are constants. The term Quadrature represents that there are only four possible phases. The general expression for a QPSK waveform as shown in equation (1), $si\ (t\ ) = A\cos[\omega c\ t + \phi 0 + \phi\ i\ (t\ )]$…….(1) where *si* represents the PSK signal waveform for phase *i t* represents time *A* represents the peak amplitude ω*c* represents the carrier frequency in radians/s ($\omega c = 2\pi fc$) $\varphi 0$ represents the reference phase angle φi represents the phase *i i* ranges from 1 to 4 The instantaneous phase having discrete values equal to $\Phi + 2\pi i/4$ where $i = 1, 2, 3,$ or 4 [10].

1.1 Quadrature Phase Shift Keying (QPSK):

The generation of the QPSK signal is usually done by modulating two carriers in Quadrature independently (cos ωt and sin ωt).

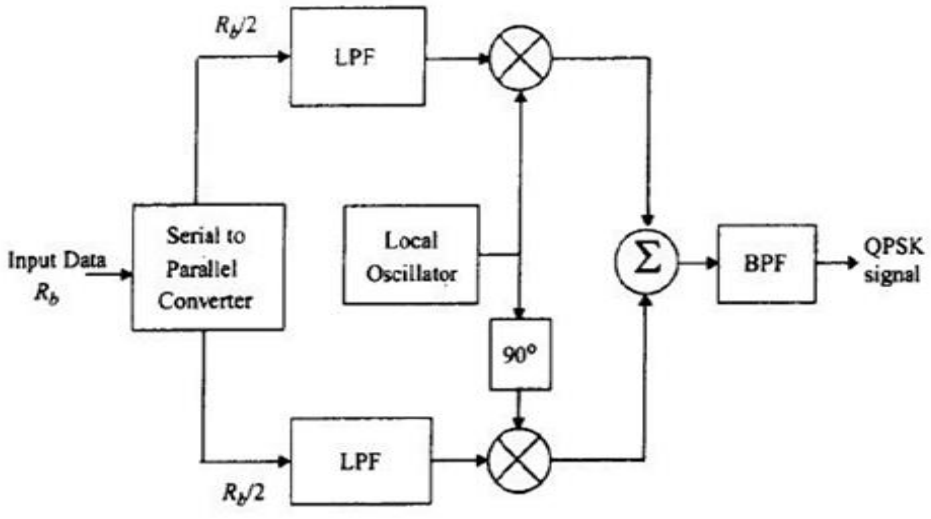

Figure 1: Simplified block diagram of a QPSK modulator.

Quadrature Phase Shift Keying is generated by two independent BPSK systems (I and Q), and exhibits the same performance but bandwidth efficiency will be double. The Serial to Parallel Converter groups as di-bits from the binary data input. Two bits have been clocked at a time serially into its buffer, the Serial to Parallel Converter outputs one di-bit in parallel at its two outputs. From the di-bit, One bit is sent to the I channel of the modulator and the other bit is sent to the Q channel of the modulator and the modulators will be working independently for each channel to processes the stream of bits it receives. In order to convert the data into a bipolar pulse stream we use Level converter the converted data is applied to one input of the mixer. A Low-Pass Filter (LPF) is usually used before the mixer in each channel of the modulator to restrict the bandwidth of the QPSK signal, in order to provide the desired spectral shaping{10].

The sinusoidal carriers of I-channel and Q-channel are cosωt and sinωt respectively, and they are in Quadrature. The modulation is performed by each mixer by multiplying the 54 carrier with the bipolar data signal in order to produce a BPSK signal. Finally two BPSK signals are summed to produce the QPSK signal. Because these two BPSK signals are generated by considering two carriers in phase Quadrature, the BPSK signals are orthogonal, and the QPSK demodulator will be able to demodulate them separately. Figure 3 shows generation of QPSK signal by two BPSK signals.

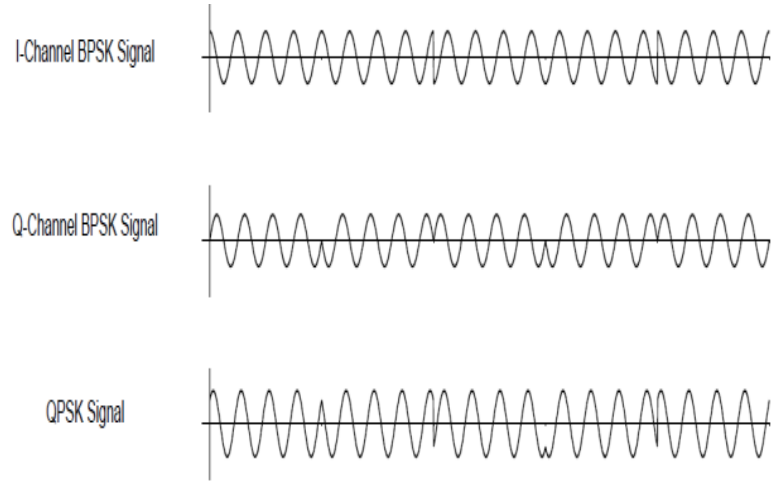

Figure 2: QPSK signal generation from two BPSK signals.

Types of QPSK:

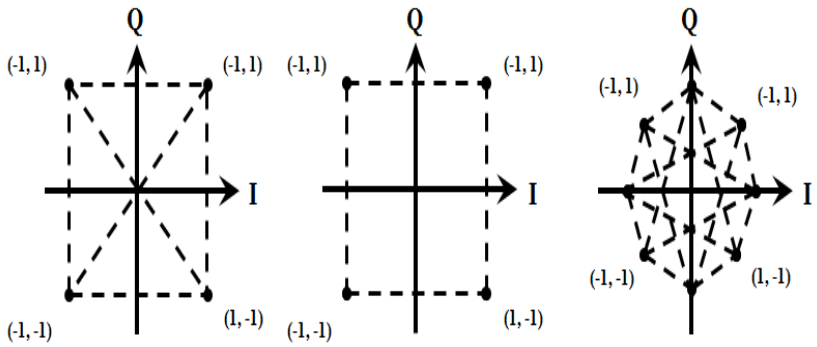

Figure 3: (a) Conventional QPSK, (b) Offset QPSK and (c) π/4 QPSK

(a) Conventional QPSK: In Conventional QPSK have transitions through zero ie. Phase transition is 1800 .

(b) Offset QPSK: In Offset QPSK the transitions are straggered on the I and Q channels. Phase transition limited to 900.

(c) π/4-QPSK: In π/4-QPSK the set of constellation points are toggled each symbol, so transitions through zero cannot occur. This scheme produces the lowest envelope variations. Where I = In phase channel, Q = Quadrature channel

1.2 Binary Phase-shift keying (BPSK) :

BPSK is a digital modulation scheme that conveys data by changing, or modulating, two different phases of a reference signal (the carrier wave).

Transmitter:-

In the analog domain, multiplying the carrier by a positive or negative DC voltage is the best method of creating a BPSK signal for this design as a square symbol will use the fewest resources. While this is an option in the digital domain, a better approach for the KUAR is to change the lookup address of a direct digital synthesizer (DDS). The DDS is an IP Core provided by Xilinx that uses two registers to determine the address of a look-up table containing the value of the sine and cosine of the argument. The two registers used to calculate the address are the phase increment and phase accumulator. The phase increment is proportional to the desired output frequency and inversely proportional to the input clock. The phase accumulator is the primary factor in the output width of the signal[11]..

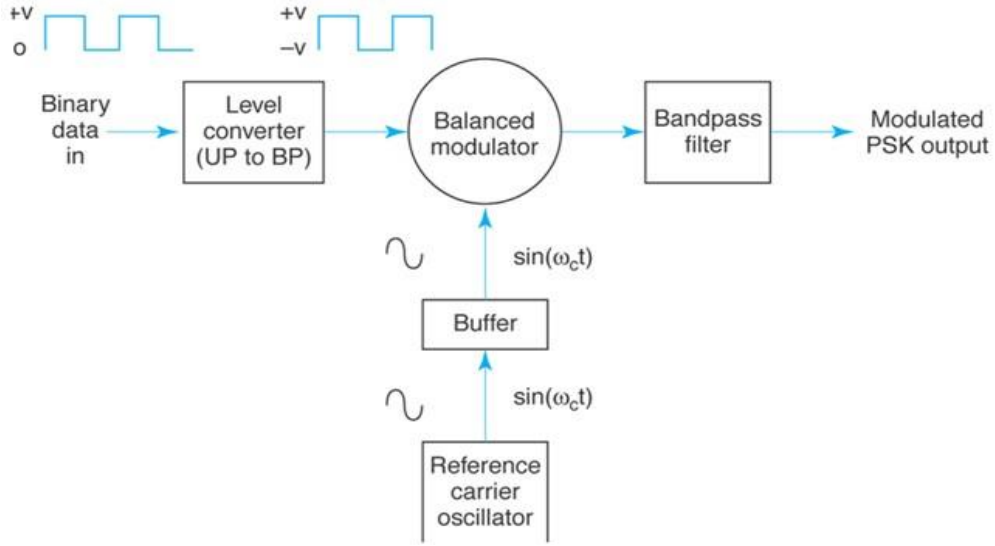

Figure 4: Block Diagram of Transmitter

Receiver:-

Given that the preferred method of receiving phase-shift-keying (PSK) signals is through a Costas loop, the analog design must be ported to the digital domain. [22] This process involves converting mixers to multipliers, analog filters to digital filters, and using DDS modules instead of local oscillators. However, the theory remains the same as his original design in 1956, which is displayed in Figure 9. [1] The first step is to demodulate the signal. Next, the signal is filtered and integrated. Then, phase tracking techniques are used to lock the receiver's carrier and phase to the transmitted signal. Simultaneously, the estimated bit pattern is aligned to the system clock. The modifications are shown in Figure 4 demonstrate the similarities between the original and modified receiver design.

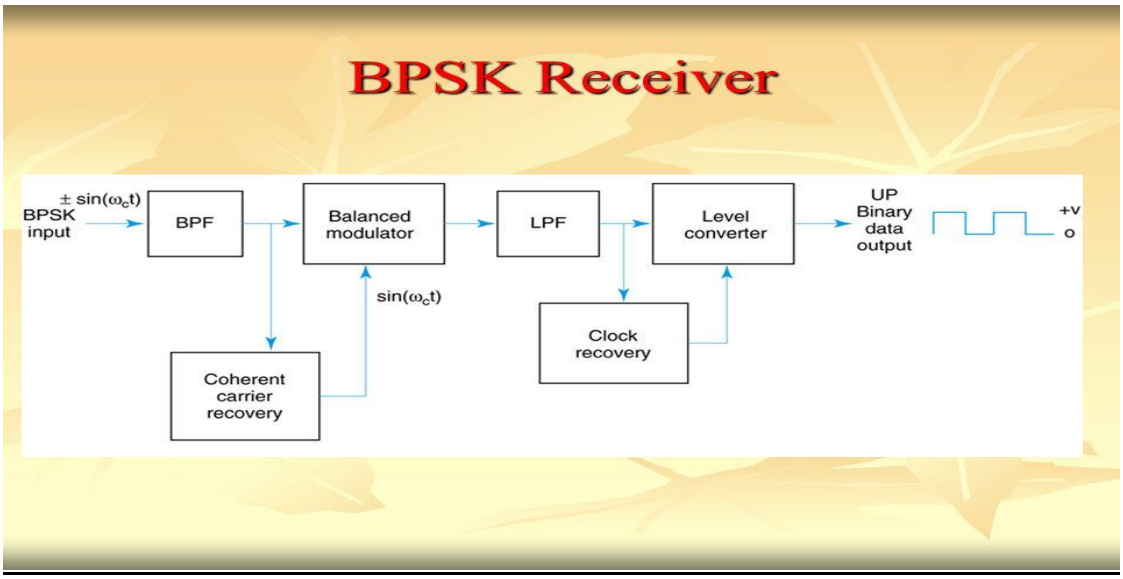

Figure-4:- BPSK Receiver

1.3 DP-QPSK (Dual Polarization Quadrature Phase Shift Keying)

It is a fiber optic digital modulation technique which uses two orthogonal polarizations of a laser beam, with QPSK digital modulation on each polarization.

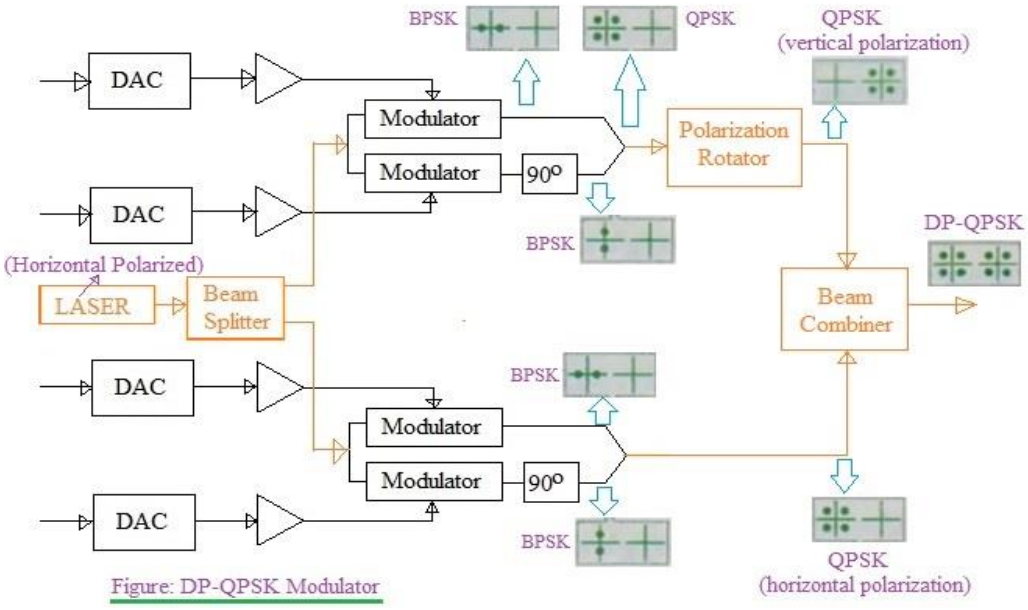

Figure-5: DP-QPSK modulator block diagram

DP-QPSK is the short form of Dual Polarization Quadrature Phase Shift Keying. The figure-3 depicts DP-QPSK modulator block diagram. DP-QPSK modulation uses two polarizations with the same original QPSK constellation to represent bits. It uses horizontal polarization and vertical polarization along with QPSK to represent information bits. In DP-QPSK, one symbol represents 4 bits in DP-QPSK compare to 2 bits in QPSK.

Laser beam in optical communication can be split into two orthogonal polarizations i.e. horizontal and vertical. DP-QPSK is digital modulation technique used in optical domain. It uses two orthogonal polarizations i.e. vertical and horizontal of the laser beam with QPSK modulation on each of these polarizations.

Let us understand how DP-QPSK modulator works as shown in the figure-3. As mentioned here laser source is linearly polarized i.e. it has only one polarization. Let us assume it is horizontally polarized. As shown power of laser source is splitted using beam splitter. Beam splitter produces two signals having same polarization and equal power. One is given to upper QPSK modulator part while the other is given to lower QPSK modulator part. In the upper part QPSK signal polarization is rotated to make vertical polarizated signal. This vertical polarized QPSK signal is combined with horizontal polarized QPSK signal from the lower part to obtain DP-QPSK modulation signal.

1.4. Pulse- width/ Duration modulation (PDM):-

PDM is a modulation process or technique used in most communication systems for encoding the amplitude of a signal right into a pulse width or duration of another signal, usually a carrier signal, for transmission.

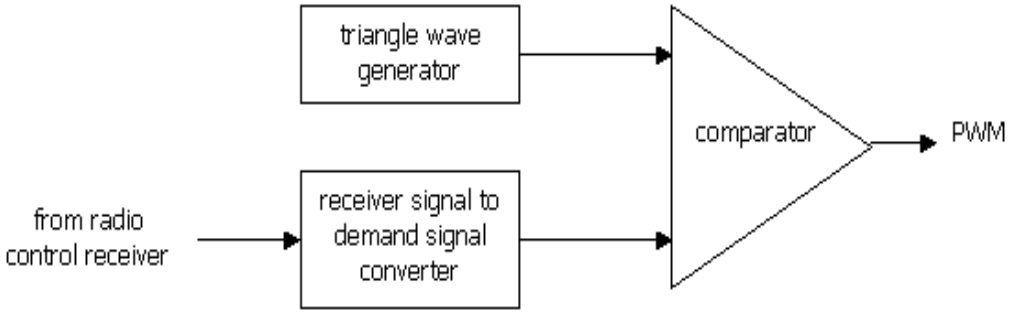

Figure-6:- Block Diagram of Pulse-Duration Diagram

The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast rate. The longer the switch is on compared to the off periods, the higher the total power supplied to the load.

The PWM switching frequency has to be much higher than what would affect the load (the device that uses the power), which is to say that the resultant waveform perceived by the load must be as smooth as possible. The rate (or frequency) at which the power supply must switch can vary greatly depending on load and application.

2. RESULTS AND WAVEFORMS

2.1 Quadrature Phase Shift Keying (QPSK):

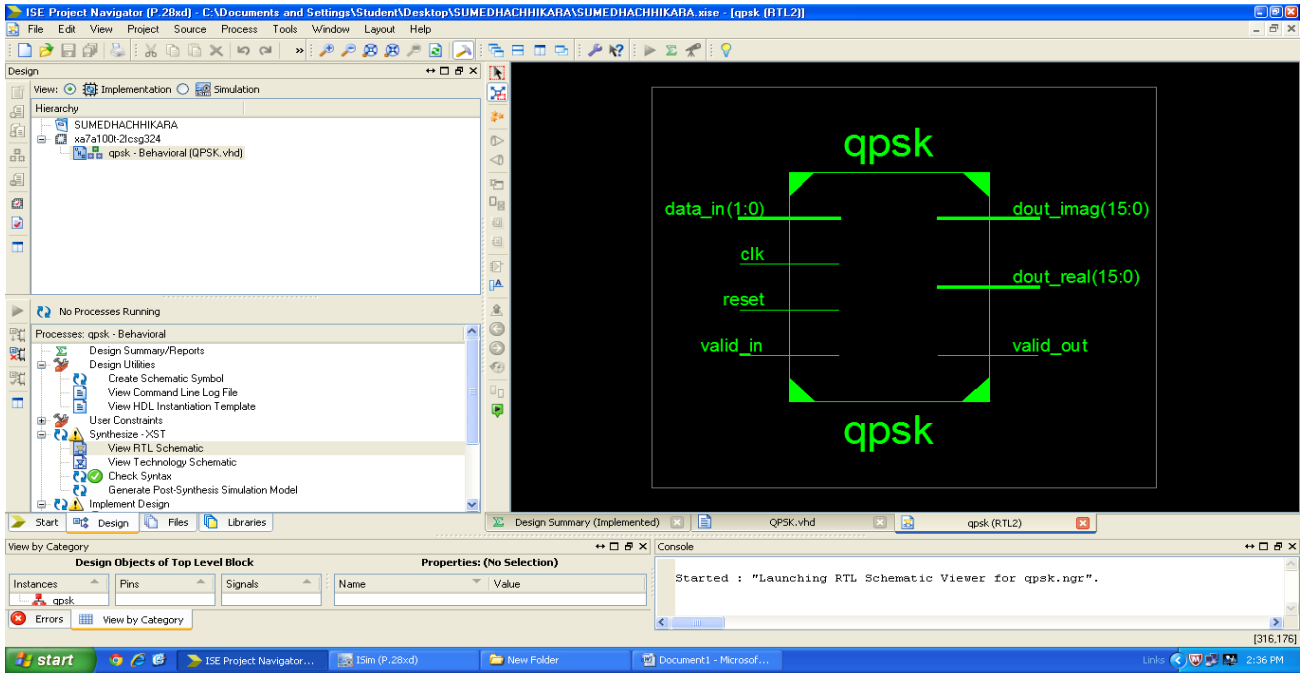

Figure-7(a):-RTL Schematic of QPSK

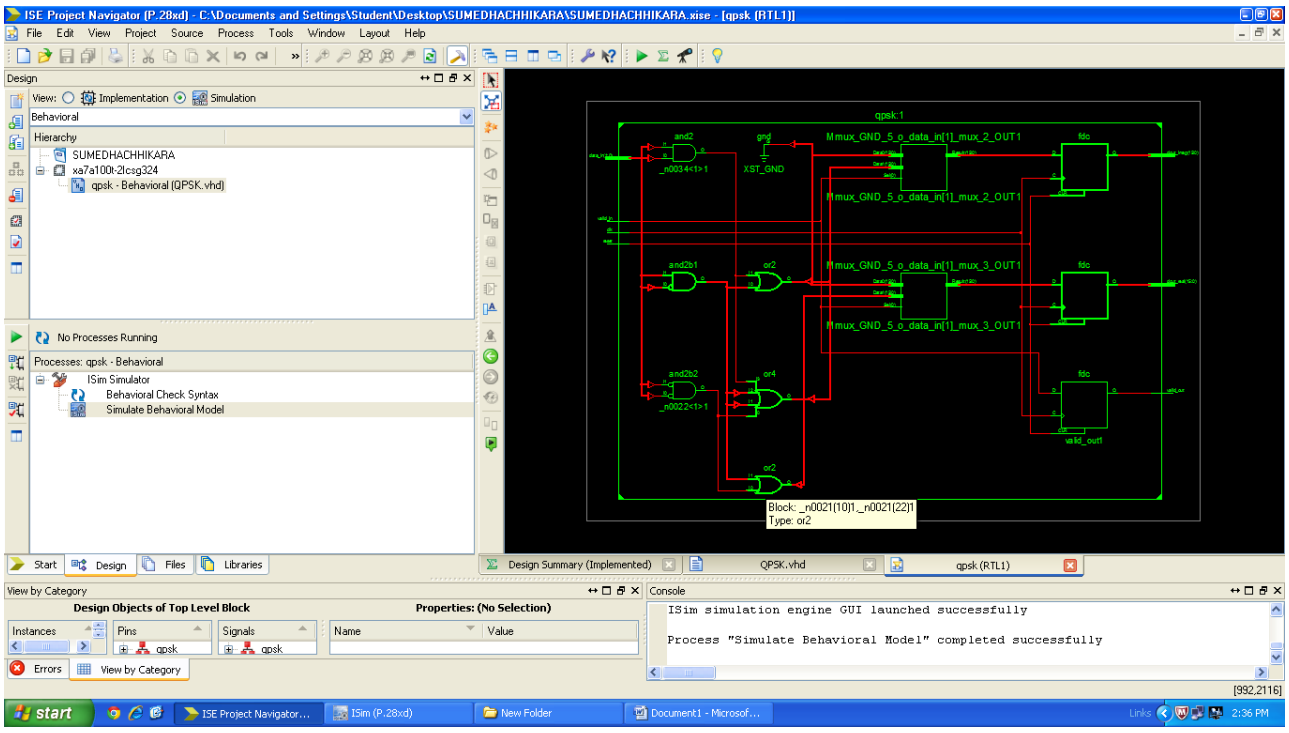

Figure-7(b):-RTL Schematic of QPSK

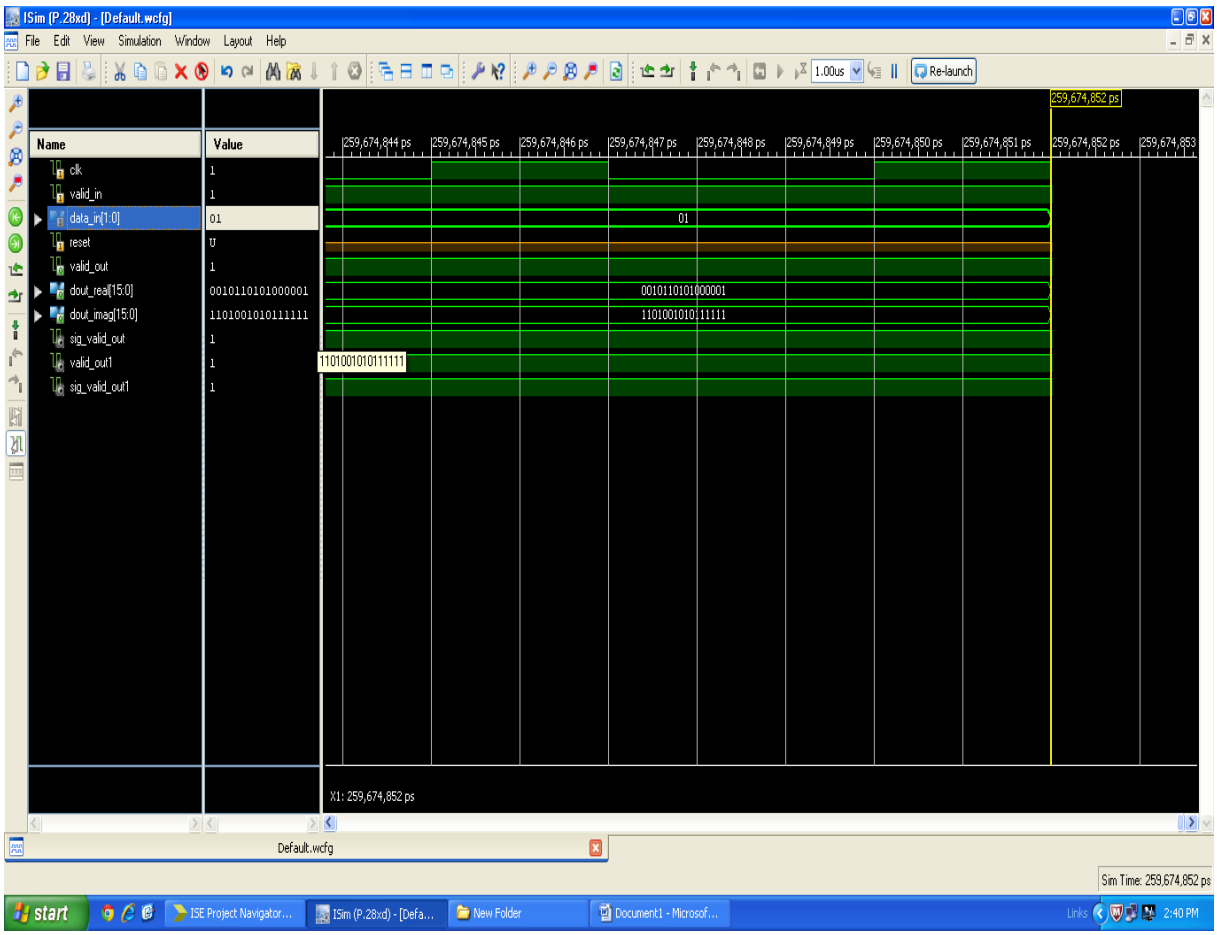

Figure-7(c):- Waveform

2.2 Binary Phase-shift keying (BPSK):

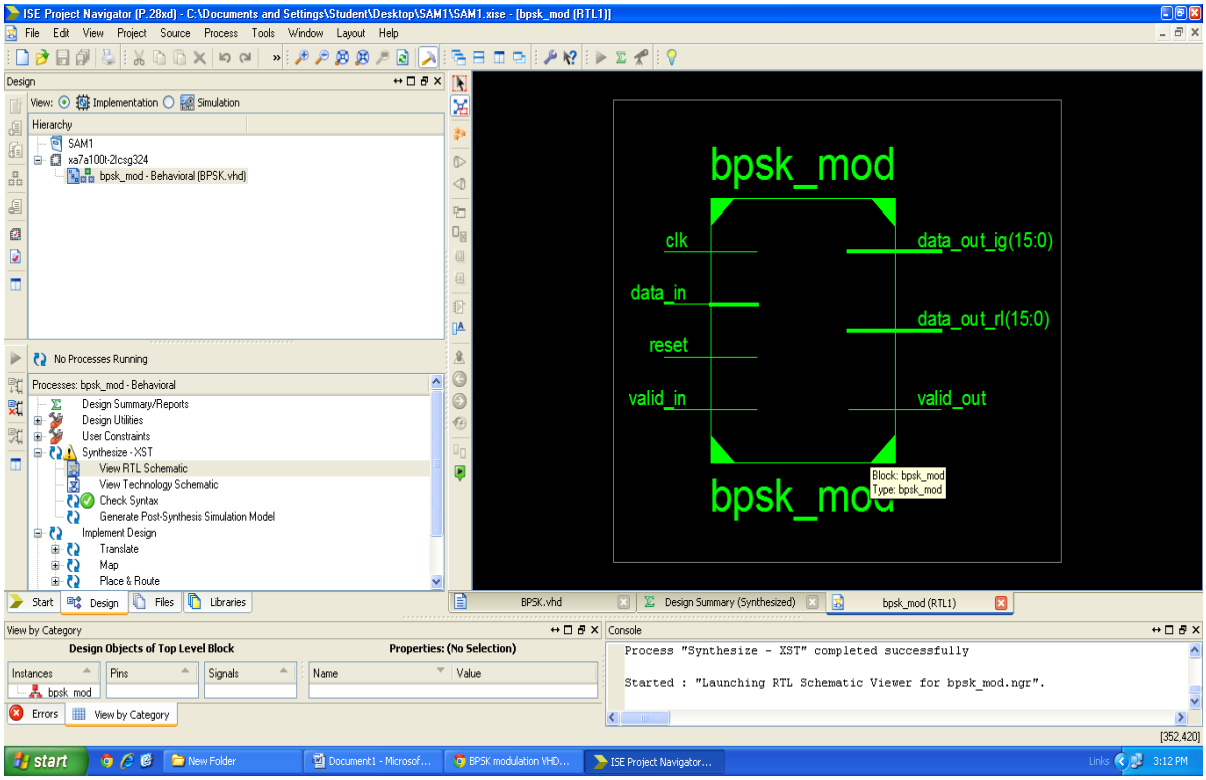

Figure-8(a):-RTL Schematic of BPSK

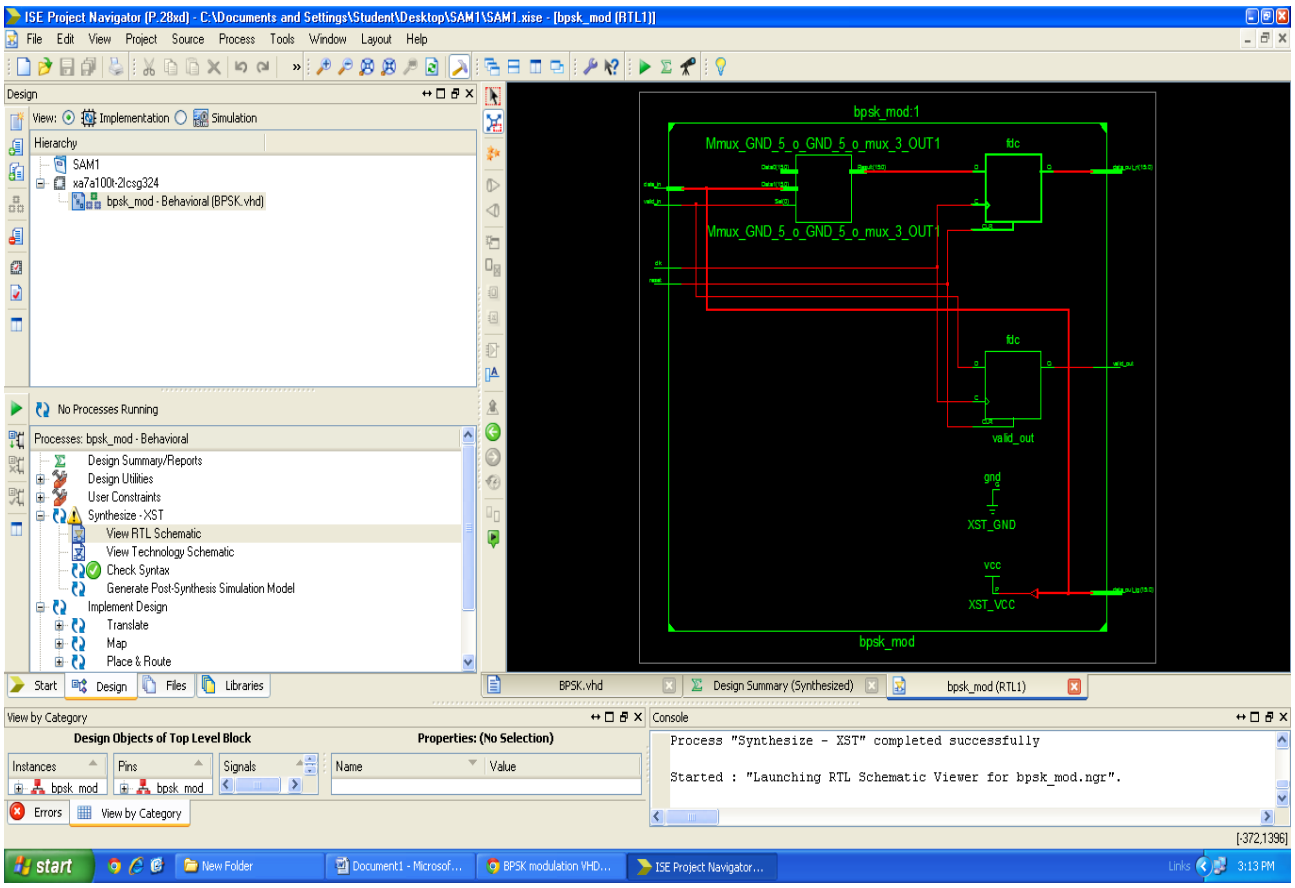

Figure-8(b):-RTL Schematic of BPSK

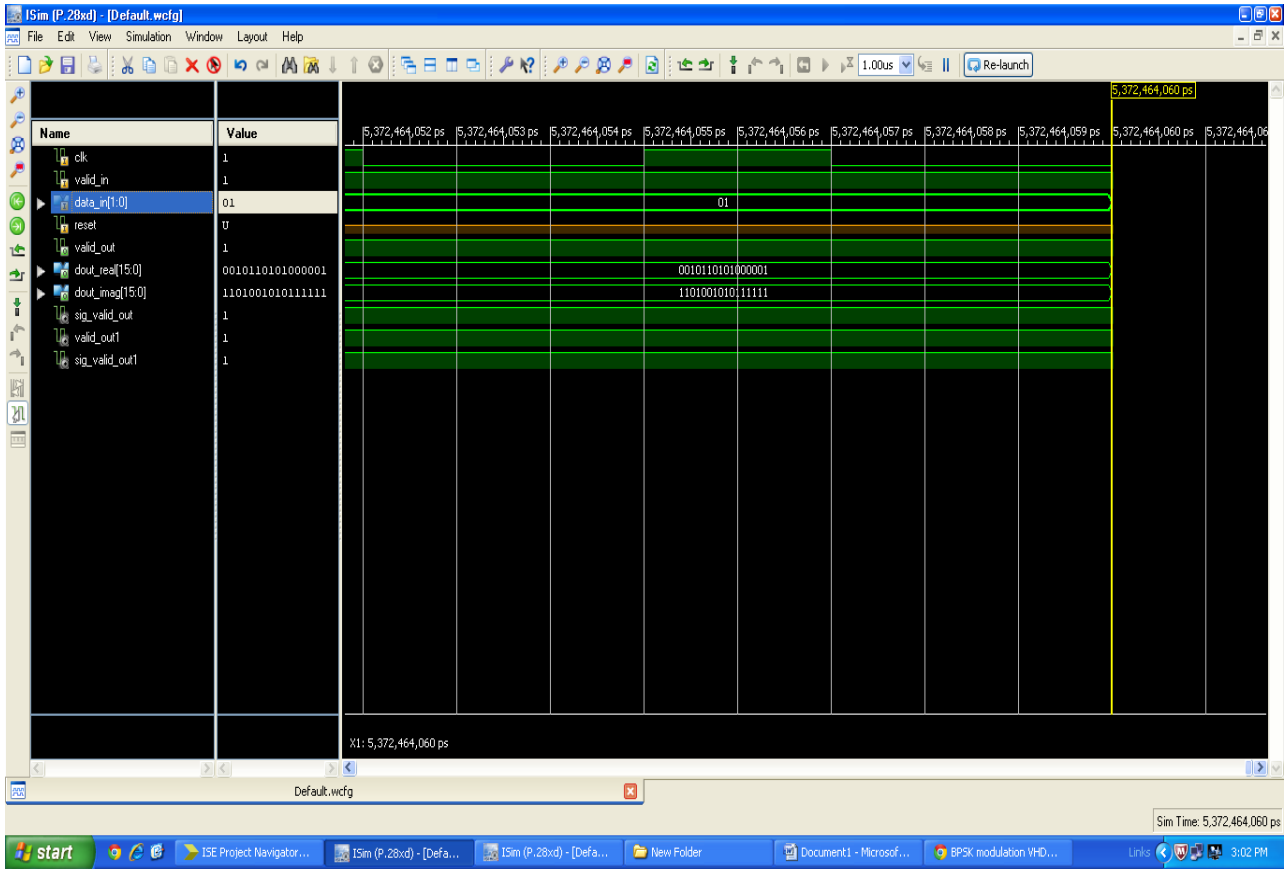

Figure-8(c): Waveform

2.3. Pulse- width/ Duration modulation (PDM):

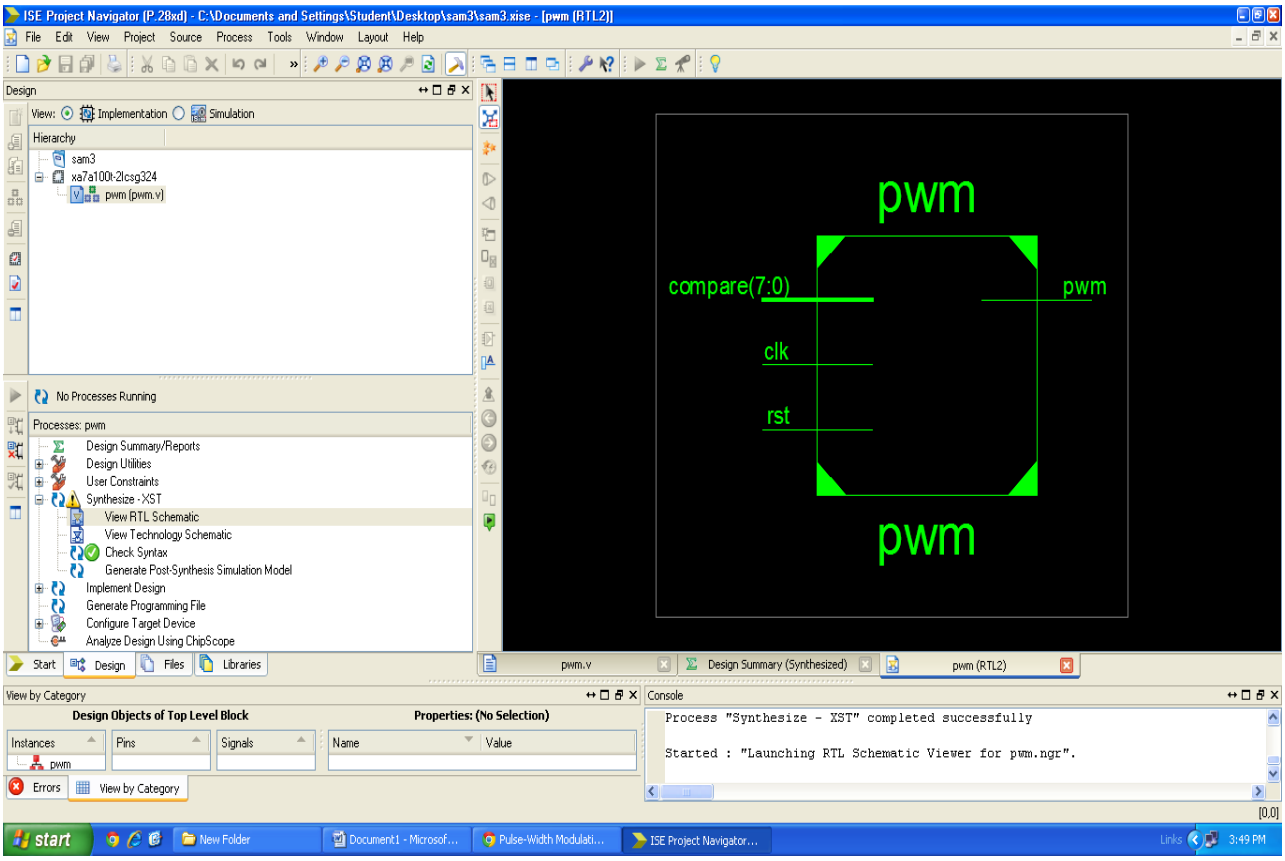

Figure-9(a):-RTL Schematic of PDM/PWM

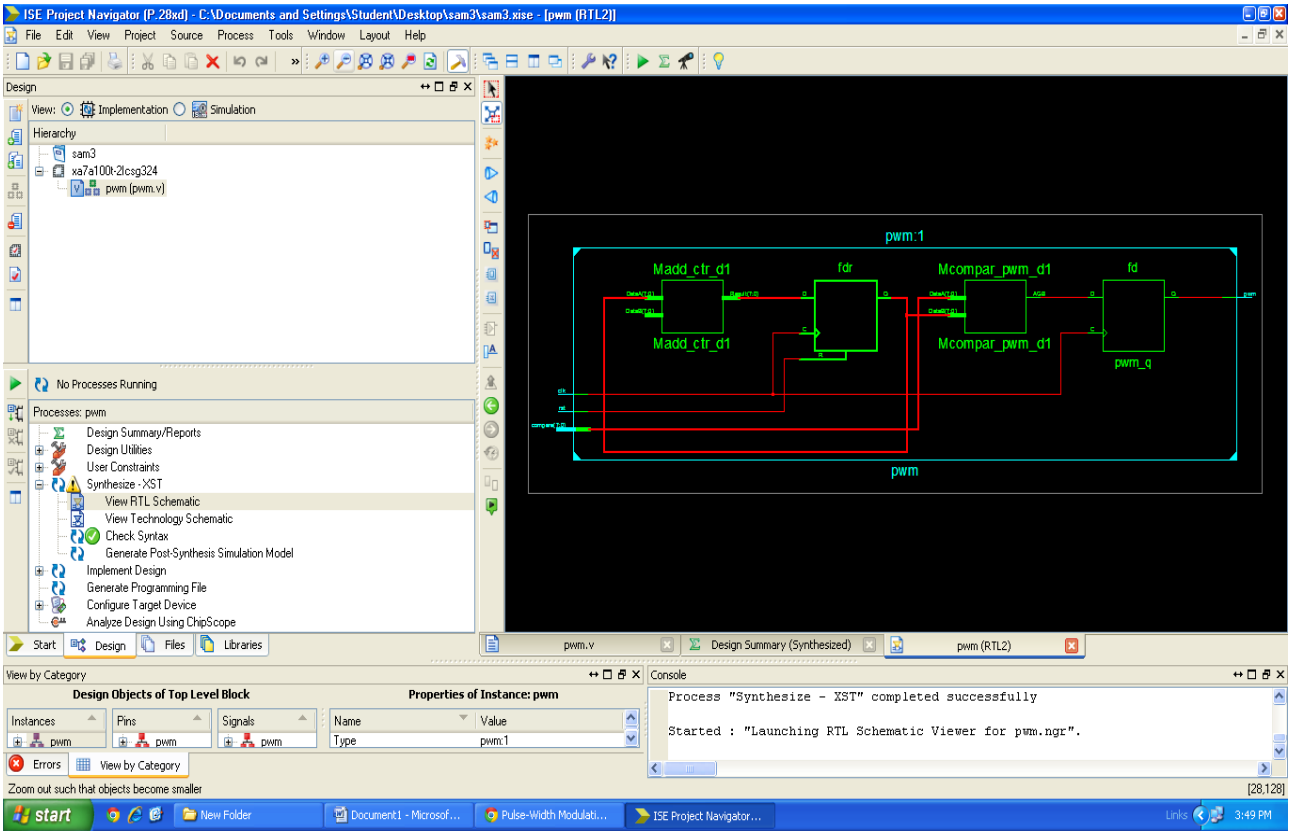

Figure-9(b):-RTL Schematic of PDM/PWM

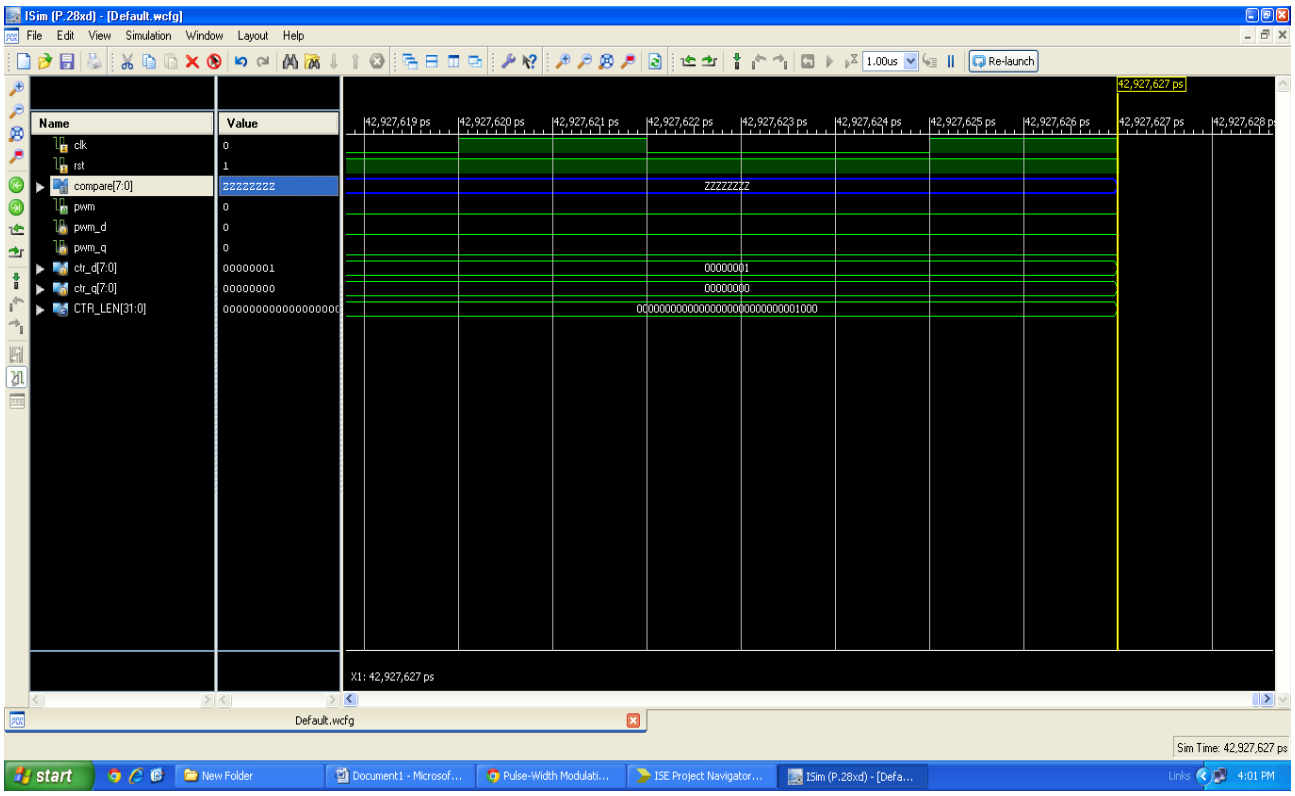

Figure-9(c):-Waveform

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